Claims:

Listing ofClaims:

This listing of claims will replace all prior versions and listings of claims in the application:

1-22. (cancelled)

23. (currently amended) An integrated circuit fabricated on a semiconductor substrate and having at least two devices, each of the devices having a different effective gate oxide thickness, the circuit comprising:

a first device having a first gate disposed on a gate dielectric layer, the gate dielectric layer having a first thickness and a first effective gate dielectric value and disposed on the semiconductor substrate;

a second device having a second gate disposed on a gate dielectric layer having the first thickness and the first effective gate dielectric value, the gate dielectric layer fabricated on a semiconductor substrate, a buried channel implanted below the gate dielectric layer, the buried channel being doped with a predetermined dopant of a first conductivity type and a peak concentration of the dopant positioned at a selected level in the substrate of a second conductivity type below the gate dielectric layer to cause the substrate portions above the selected level to act as a supplemental gate dielectric layer to increase the effective gate dielectric thickness of the second device, wherein the level is selected so that the effective gate dielectric thickness of the second device is a predetermined value greater than the first effective gate dielectric value.

24. (previously added) The integrated circuit as recited in claim 23 wherein the insulating gate dielectric layer and the substrate forms an interface and the peak concentration of implanted dopants in the buried channel is located between 400 and 1000 Angstroms below the interface.

25. (previously added) The integrated circuit as recited in claim 23 wherein the device is a MOS capacitor.

C1

26. (previously added) The integrated circuit as recited in claim 23 wherein the substrate is a p-type substrate and the buried channel is an n-type buried channel.

C2

27. (new) The integrated circuit as recited in claim 23 wherein the substrate is a n-type substrate and the buried channel is an p-type buried channel.

28. (new) The integrated circuit as recited in claim 23 wherein the second device is configured cause the substrate portions above the selected level to act as a supplemental gate dielectric layer when the second gate is biased with respect to the substrate and the buried channel is partially depleted of charge carriers, effectively increasing the thickness of the insulating gate dielectric layer.

29. (new) The integrated circuit as recited in claim 23 wherein the first device has a threshold voltage implant having the same concentration and conductivity type as the predetermined dopant formed beneath the second gate and is formed in a substrate of the first conductivity type.

30. (new) The integrated circuit as recited in claim 23 wherein the first gate is doped with a first conductivity type impurity and the second gate is doped with a second conductivity type impurity.

31. (new) The integrated circuit as recited in claim 23 wherein the first gate is doped with a second conductivity type impurity and the second gate is doped with a first conductivity type impurity..